ABSTRACT

**LOW COST, HIGH PERFORMANCE FLIP CHIP PACKAGE STRUCTURE**

A chip scale integrated circuit chip package includes a die mounted by flip chip interconnection to a package substrate. The package substrate is a laminate including a dielectric layer having a single conductive trace layer on a first surface thereof (the "circuit side" of the substrate) and an active ground plane overlying a second surface thereof (the "dielectric side" of the substrate), wherein the die is mounted on the circuit side of the dielectric layer, the ground plane is electrically connected to ground sites at the first surface of the dielectric layer through openings in the dielectric layer, and wherein second level interconnects are on the circuit side of the dielectric layer. Also, methods for making the package include providing a substrate that includes a laminate including a dielectric layer having a single conductive trace layer on a first surface thereof (the "circuit side" of the substrate) and an active ground plane overlying a second surface thereof (the "dielectric side" of the substrate); affixing a die onto the circuit side of the substrate and forming thereon a flip chip interconnection; filling the vias with an electrically conductive material; applying a ground plane material onto the dielectric side of the substrate; and curing the electrically conductive fill material to form electrical connection between the ground plane and ground sites on the conductive trace layer.